IN THE CLAIMS

1. (currently amended) A method for producing yield enhancement data for integrated circuits on a substrate, the method comprising the steps of:

comparing a database of physical defects on the substrate to a database of design information for the integrated circuits, and

associating the defects on the substrate with classes of design information by location on the substrate of both the defects and elements of the design information to produce the yield enhancement data.

2. (original) The method of claim 1, wherein the database of defects comprises a defect wafer map.

3. (original) The method of claim 1, wherein the defects on the substrate are optically observable defects.

4. (original) The method of claim 1, wherein the design information includes structures formed in the integrated circuits.

5. (original) The method of claim 1, wherein the classes of design information comprises classes of physical structures.

6. (original) The method of claim 1, further comprising the step of creating the database of defects by inspections of the substrate, where the inspections are conducted at multiple times during fabrication of the integrated circuits.

7. (original) The method of claim 1, further comprising the step of creating the database of design information from design files for the integrated circuits.

8. (original) The method of claim 1, further comprising the step of revising the design information based at least in part on the yield enhancement data.

9. (currently amended) A method for producing yield enhancement data from integrated circuits on a substrate, the method comprising the steps of:

PAGE 2/10 * RCVD AT 10/27/2005 4:08:17 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:1.865.934.0444 * DURATION (mm-ss):07-04

creating a database of design information for the integrated circuits, which design information is used as a template for fabricating the integrated circuits, where the design information includes structure location information for physical structures used to form the integrated circuits,

binning the structures in the design information in the database of design information as belonging to at least one of a number of different classes of physical structures,

creating a database of physical defects on the substrate during inspections of the substrate that are conducted during processing of the integrated circuits, where the defects listed in the database of defects are associated with defect location information,

comparing the database of design information with the database of defects to create associations between the design information and the defects based on matching the structure location information with the defect location information, and

~~associating the database of defects with the database of design information by physical proximity of~~ reporting the defects based on the ~~to~~ classes of the design information with which they are associated as a result of the comparison, to produce the yield enhancement data.

10. (original) The method of claim 9, wherein the database of defects comprises a defect wafer map.

11. (original) The method of claim 9, wherein the defects on the substrate are optically observable defects.

12. (canceled)
13. (canceled)
14. (canceled)

15. (original) The method of claim 9, further comprising the step of revising the design information based at least in part on the yield enhancement data.

PAGE 3/10 * RCVD AT 10/27/2005 4:08:17 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:1.865.934.0444 * DURATION (mm-ss):07-04

16. (currently amended) A computerized system for analyzing defects, the system comprising:

means for receiving design information for integrated circuits, where the integrated circuits are fabricated on a substrate based on the design information, where the design information includes structure location information for physical structures used to form the integrated circuits,

means for binning the structures in the design information in the database of design information as belonging to at least one of a number of different classes of physical structures,

means for receiving physical defect information for integrated circuits, where the defect information contains locations of defects on the substrate,

means for comparing the design information with the defect information based on matching the structure location information with the locations of defects on the substrate, and

means for associating the defects with the classes of the design information based on physical proximity on the substrate to produce yield enhancement data.

17. (original) The system of claim 16, wherein the defect information comprises a defect wafer map.

18. (original) The system of claim 16, further comprising means for revising the design information based at least in part on the yield enhancement data.

19. (canceled)

20. (canceled)

PAGE 4/10 * RCVD AT 10/27/2005 4:08:17 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/28 * DNIS:2738300 * CSID:1.865.934.0444 * DURATION (mm-ss):07-04